R20 Regulation *Subject code: 3P4BB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech IV Semester Supplementary Examinations, June 2026

DIGITAL ELECTRONICS

(EEE)

Maximum Marks: 70 Date: 10.06.2026 Duration: 3 hours

Note: **1. This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

	All the following questions carry equal marks (10X2M=20 Marks)	Marks	CO	BTL
1	Convert the following to the required form. i)$(11001.001)_2$=( )$_{10}$ ii) $(126)_8$=( )$_{10}$	2M	1	L1
2	Convert binary value 1011010 to gray value?	2M	1	L1
3	State and Prove De-Morgan's theorem.	2M	2	L1
4	Simplify the Boolean function F(X,Y,Z)=$\sum$m(3,4,6,7) using K-map.	2M	2	L1
5	Design full adder using two half adders	2M	3	L1
6	Difference between Static Hazards and Dynamic Hazards?	2M	3	L1
7	Convert JK Flip Flop to T Flip Flop	2M	4	L1
8	What are applications of Ring counters?	2M	4	L1
9.	Define Finite State Machine	2M	5	L1
10	What is a state diagram?	2M	5	L1

Part-B

	Answer All the following questions. (5X10M=50Marks)	Marks	CO	BTL
11	a) Encode the message bits $(1110)_2$ into 7-bit even parity hamming code. b) Given that $(81)_{10} = (100)_b$, Find the value of b.	5M 5M	1	L2
	OR			
12	a) Convert $(736)_{10}$=( )$_2$, ( )$_8$, ( )$_{16}$ b) Add the BCD addition of 204.6+185.5	5M 5M	1	L2
13	Simplify the following expression using tabulation method y(w,x,y,z)=$\sum$m(1,2,3,5,6,7,8,9,12,13,15)	10M	2	L2
	OR			
14	Minimize the following expression using K-map and realize using NOR Gates f =πM(0,4,6,7,8,12,13,14,15).	10M	2	L2
15	Design a Full adder using two Half adders and realize the NAND realization of Full adder?	10M	3	L2
	OR			
16	Explain the differences between MUX and DEMUX. Realize 16-input multiplexer by using 8-input multiplexers.	10M	3	L2

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<tr><td>17</td><td>Explain the realization of SR flip-flop using D flip-flop.</td><td>10M</td><td>4</td><td>L2</td></tr>
<tr><td></td><td>OR</td><td></td><td></td><td></td></tr>
<tr><td>18</td><td>Design a MOD-10 ripple counter.</td><td>10M</td><td>4</td><td>L2</td></tr>
<tr><td>19</td><td>A clock mode sequential circuit has to provide z=1 whenever the input completes the Sequence of pulses 1010 and overlapping is allowed. Draw the state diagram and obtain minimal state using partition method.</td><td>10M</td><td>5</td><td>L2</td></tr>
<tr><td></td><td>OR</td><td></td><td></td><td></td></tr>
<tr><td>20</td><td>Draw the merger graph and obtain the set of Maximal compatibles for the incompletely specified sequential machine for given state table.
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<tr><td>PS</td><td colspan="2">NS,Z</td></tr>
<tr><td></td><td>I1</td><td>I2</td></tr>
<tr><td>A</td><td>E,0</td><td>B,0</td></tr>
<tr><td>B</td><td>F,0</td><td>A,0</td></tr>
<tr><td>C</td><td>E,--</td><td>C,0</td></tr>
<tr><td>D</td><td>F,1</td><td>D,0</td></tr>
<tr><td>E</td><td>C,1</td><td>B,0</td></tr>
<tr><td>F</td><td>D,--</td><td>B,0</td></tr>
</table></td><td>10M</td><td>5</td><td>L2</td></tr>
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